Eliot Abramo

Embedded Systems Engineer | Space Hardware–Software Co-design | FPGA and Analog Systems

eliot.abramo@epfl.ch | +41 78 258 03 70 | Portfolio | LinkedIn

Embedded systems engineer focused on reliable space hardware–software co-design. Flight-tested electronics for orbital payloads (launch scheduled March 2026). European Space Robotics Champion 2025.

Experience

Embedded Systems Engineer – Space Payloads, SpaceLocker, Toulouse, France **Sep. 2025 – Present**

Flight hardware–software development for orbital payload systems

- Developed an automated ECSS-compliant reliability-tracing tool integrated into KiCad, providing end-to-end traceability from schematic/BOM to ECSS reliability budgets and informing design trade-offs early in the design cycle.
- Designed, built and tested electronics for space payload systems scheduled for orbital deployment in March 2026, including power conditioning, data handling and watchdog/safing circuitry.
- Participated in official ESA PDR and CDR processes: assembled data packages, justified system design choices and iterated based on formal feedback.
- Designed an analog-logic safety board with voting logic, watchdogs and safe-mode fallbacks to ensure autonomous recovery from satellite anomalies, including dead-on-arrival scenarios.
- Contributed to space qualification testing: TVAC campaigns, vibration and shock testing, functional and integration tests, and end-to-end system validation.
- Wrote flight software in C and Rust under ECSS constraints, using MISRA-inspired coding practices for fault-tolerant communication, on-board diagnostics and telemetry handling.

Lead System Engineer, EPFL Xplore Rover, EPFL **Aug. 2024 – Sep. 2025**

1st Place – Space Robotics Champions, European Rover Challenge 2025

- Led the electronics and embedded systems side of the rover that won ERC 2025, working across avionics, power, communications, perception and ground segment.
- Coordinated rover system architecture within a large multidisciplinary team, owning electrical and communication interfaces between STM32/ESP32-based avionics, sensors, actuators and the operator station.
- Designed and implemented a full custom avionics communication stack: deterministic SPI interconnect with UART failover, zero-copy circular buffers and CRC framing used as the main inter-node bus during ERC operations.
- Built a full-duplex communication bridge linking avionics nodes to a ROS 2 network, using custom-framed packets with explicit CRC error checking and type-safe dispatch between embedded and Linux domains.
- Set up hardware-in-the-loop testbeds and regression test harnesses for avionics and communication stacks to catch integration issues before field tests and competition runs.

Research Assistant, Laboratory of Wave Engineering (LWE), EPFL **Sep. 2024 – Aug. 2025**

- Led an independent research project on "Nonlinear activation functions for analog neurons in low-power deep learning applications," exploring physical nonlinearities for analog accelerators under the guidance of a PhD researcher.
- Built and characterized a tunable 2.4 GHz binary metasurface using coupled resonators with PIN-diode control for programmable RF wavefront manipulation.
- Prototyped an optical GELU-like activation using structured incoherent light and Fresnel propagation as a primitive for optical neural networks.
- Co-designed simulations and experiments using CST Studio Suite, vector network analyzers and Python/C++ processing pipelines.

Embedded Systems Engineer, EPFL Xplore Rover, EPFL **Sep. 2023 – Aug. 2024**

- Designed and manufactured custom PCBs for STM32 and ESP32 avionics with attention to power efficiency, signal integrity and robustness to outdoor competition conditions.
- Implemented and maintained communication stacks over CAN, SPI, I^2C and UART, including CRC validation, zero-copy buffers and graceful handling of link failures.
- Developed and used a custom CAN MessageBus framework for static, zero-overhead packet exchange across rover subsystems, with packed packet definitions and protocol versioning.
- Contributed to lower- and higher-level system pipelines in ROS 2, helping integrate avionics data into autonomy and operator tools.

Head of Communication, IEEE EPFL Student Branch **Sep. 2023 – Aug. 2024**

- Managed communication strategy and content, increasing student engagement by around 30%.
- Organized the 2023 IEEExtreme Hackathon and industry visits, connecting students with engineering teams in industry.

Research Assistant, American University in Dubai (AUD) **Dec. 2020 – Jan. 2022**

- Assisted on projects involving blockchain integration for IoT systems and microgrid/renewable energy research in collaboration with the University of New Mexico.

Selected Technical Projects

- **Custom ROS 2 ↔ Embedded MCU Bridge** – Full-duplex hardware-agnostic communication bridge between ROS 2 and bare-metal microcontrollers using custom CRC-framed packets. Target implementation over UART/SPI, providing reliable, high-throughput telemetry and command channels between Linux and embedded nodes.
- **Full Custom Avionics Communication Stack** – Deterministic SPI layer with UART failover, zero-copy circular buffers and CRC validation, forming the main real-time inter-node messaging backbone in the EPFL Xplore avionics.
- **SpaceEther** – Lightweight custom transport protocol running on raw Ethernet or UDP, offering framing, optional forward error correction and authentication, and topic-oriented payloads for embedded "black boxes" talking directly to standard PCs or ROS 2 systems without extra PC-side software.
- **FPGA + ARM Radio Astronomy Accelerator** – Implemented an FPGA accelerator on a Zynq-7020 (PYNQ-Z2) that converts raw radio telescope data, extracting Doppler-shifted 21 cm hydrogen lines to estimate Milky Way rotation. Developed using a hardware-software co-design process with optimized hardware accelerators.
- **CNN FPGA Accelerator** – Designed and optimized a 3×3 convolution accelerator in Vitis HLS for a CNN that classifies dog and cat images on a Zynq-7020 (Pynq-Z2). Implemented coefficient caching, multi-row input buffering and parallel filter computation to cut external memory accesses and improve latency over the software-only baseline, with the accelerator integrated into the Linux application running on the ARM cores.

Education

École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

- MSc in Electrical and Electronic Engineering – Specialization in Microelectronics 2025 – Present
- BSc in Electrical and Electronic Engineering (Bilingual: English/French) 2022 – 2025

Jumeirah English Speaking School (JESS), Dubai, UAE **2018 – 2022**

- International Baccalaureate Diploma: **43/45**.
- Extended essay: "How effective are Lagrange polynomials and Fourier series in modeling the spread of COVID-19 in the UK?"

Competitions and Awards

- **European Rover Challenge 2025** – 1st Place, Lead System Engineer for the winning Mars rover team.
- **4x4 in Schools, UAE** – Top 13 nationally; Innovation Award for suspension and obstacle navigation design.
- **First Lego League (FLL) Robotics** – Design and Innovation Award 2020 (250+ teams); Top 10 in 2018 (300+ teams).
- **UN Geneva Forum Presenter** – Presented an ecological sensing device project, highlighting the use of embedded electronics in environmental research.

Technical Skills

- **Space Systems:** ECSS standards, TVAC testing, vibration/shock testing, PDR/CDR workflows, redundancy/safing design, basic EMC/EMI considerations.
- **Programming:** C, C++, Rust, Python (OpenCV, ROS 2, PyTorch), VHDL, MATLAB, Bash, Julia, Java, JavaScript.
- **Embedded & FPGA:** STM32, ESP32, Zynq/PYNQ, Zephyr and FreeRTOS, CAN, SPI, I^2C, UART, HIL/SIL testing.
- **Tools:** Vivado/Vitis HLS, KiCad, CST Studio Suite, Git, STM32CubeIDE, Linux, Fusion 360.
- **Languages:** English (fluent), French (fluent), Spanish (conversational).