Eliot Abramo

Embedded Systems Engineer | Space Hardware–Software Co-design | FPGA, CGRA and Real-Time ML

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Embedded systems engineer: flight-qualified space payloads, real-time ML on CERN's CMS trigger, reconfigurable compute research. European Space Robotics Champion 2025.

Education

École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

- MSc in Electrical and Electronic Engineering – Specialization in Microelectronics — 2025 – Present
- BSc in Electrical and Electronic Engineering (Bilingual: English/French) — 2022 – 2025

Jumeirah English Speaking School (JESS), Dubai, UAE — 2018 – 2022

- International Baccalaureate Diploma: **43/45**. Extended essay: Fourier series and Lagrange polynomials for modeling COVID-19 spread.

Experience

FPGA Engineer – CMS Level-1 Trigger, DAQ Team, CERN openlab, Switzerland Jun. 2026 – Aug. 2026

- Designed the custom clock-domain-crossing FIFO bridging AXI4-Stream input and the AI Engine array for AMD ACAP Versal FPGA.
- Built cycle-accurate, in-hardware latency probes across the full PL-to-AIE pipeline.
- Replaced simulated data generation with live optical-transceiver I/O, added PCIe-based external host control, and repurposed the freed PS for telemetry and health monitoring.

Research Assistant – CGRA Toolchain, ESL / SEAMS, EPFL Mar. 2026 – Jun. 2026

- Built core pieces of HELIOS, a CGRA toolchain for the Square Kilometre Array: compiler, IDE, CLI and a Python DSE library.
- Presented a research poster at SwissChips 2026 on CGRA programmability and energy efficiency.

Embedded Systems Engineer – Space Payloads, SpaceLocker, Toulouse, France Sep. 2025 – Mar. 2026

Flight hardware–software development for orbital payload systems

- Built a KiCad-integrated ECSS reliability-tracing tool – schematic to BOM to reliability budget, automatically.
- Designed, built and tested payload electronics for a March 2026 orbital launch.
- Cleared official ESA PDR and CDR reviews, defending the payload design against formal panel feedback.
- Designed an analog safety board that recovers autonomously from dead-on-arrival satellite failures.
- Wrote flight software in C and Rust; passed TVAC, vibration and shock qualification testing.

Research Assistant, Laboratory of Wave Engineering (LWE), EPFL Sep. 2024 – Aug. 2025

- Led independent research on physical nonlinearities as analog neuron activations, under Prof. Romain Fleury.
- Built and characterized a tunable 2.4 GHz metasurface for programmable RF wavefront control.
- Prototyped an optical GELU-like activation using structured light and Fresnel propagation.

Lead System Engineer, EPFL Xplore Rover, EPFL Aug. 2024 – Sep. 2025

1st Place – Space Robotics Champions, European Rover Challenge 2025

- Led electronics and embedded systems for the rover that won ERC 2025.
- Architected the rover's electrical and communication interfaces across a 120-person, multidisciplinary team.
- Built the deterministic SPI bus – UART failover, zero-copy buffers, CRC framing – that ran ERC 2025.
- Bridged avionics to ROS 2 with a full-duplex, CRC-checked link that carried live telemetry during ERC 2025.

Embedded Systems Engineer, EPFL Xplore Rover, EPFL Sep. 2023 – Aug. 2024

- Designed and manufactured custom STM32/ESP32 avionics PCBs for outdoor competition conditions.
- Built CRC-validated, zero-copy comms stacks across CAN, SPI, I^2C and UART for rover avionics.
- Built a zero-overhead CAN MessageBus framework for rover-wide packet exchange.

Selected Technical Projects

- **POLARIS + NOVA – Multi-FPGA Satellite Compute Platform.** Dual-FPGA compute platform on Zynq UltraScale+ – POLARIS handles payload data, NOVA provides reconfigurable compute, linked over a custom SpaceWire-inspired fabric.
- **Astrorapide – FPGA+ARM Radio Astronomy Accelerator.** FPGA+ARM accelerator on a Zynq-7020 that extracts hydrogen-line data in real time to map the Milky Way's rotation curve.
- **SpaceEther – Lightweight Embedded Transport.** Custom transport over raw Ethernet/UDP – framing, FEC, authentication – no middleware required.
- **Nexus – ROS 2 ↔ MCU Bridge.** Full-duplex ROS 2 ↔ MCU bridge over UART/SPI with CRC-framed packets.

Competitions and Awards

- **European Rover Challenge 2025** – 1st place overall, Drone Excellency Award.
- **Young Founders Summit Asia 2019** – Top 9 of 600+ teams; designed a MOSFET 7× smaller than commercial parts.
- **4x4 in Schools, UAE** – Top 13 nationally, Innovation Award, Yas Marina finals.

Technical Skills

- **Space Systems:** ECSS standards, TVAC/vibration/shock testing, PDR/CDR, redundancy and safing design, basic EMC/EMI.
- **Reconfigurable Hardware:** CGRA toolchain (ASTRA, Compigra), FPGA HW–SW co-design (Zynq/PYNQ, Vivado, Vitis HLS), AXI4-Stream and CDC design, ML inference on AMD Versal ACAPs.
- **Programming:** C, C++, Rust, Python (PyTorch, NumPy, ROS 2), VHDL, MATLAB, Julia, Bash.
- **Embedded and FPGA:** STM32, ESP32, Zynq/PYNQ, Zephyr/FreeRTOS, CAN, SPI, I^2C, UART, HIL/SIL testing.
- **RF and Analog:** Metasurface design, phased-array beamforming, VNA characterization, CST Studio Suite, LTSpice.
- **Tools:** KiCad, Git, STM32CubeIDE, Linux, Fusion 360.
- **Languages:** English (fluent), French (fluent), Spanish (conversational).